APPLICATION FOR REISSUE OF

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Title: FLAT PANEL DEVICE AND DISPLAY DRIVER WITH ON/OFF POWER CONTROLLER USED TO PREVENT DAMAGE TO THE LCD

FLAT DEVICE AND DISPLAY DRIVER WITH ON/OFF POWER CONTROLLER USED TO PREVENT DAMAGE TO THE LCD

This is a Divisional of prior application Ser. No. 08/267,103 filed on Jun. 23, 1994 now U.S. Pat. No. 5,563,624 which is a continuation of Ser. No. 07/834,295 filed on Apr. 9, 1992 which is now abandoned, which is a 371 of PCT Internatonal Application No. PCT/JP91/00785, filed Jun. 11, 1991, and which designated the U.S.

BACKGROUND OF THE INVENTION

1. Technical Field

The present invention relates generally to a flat display such as liquid crystal display (LCD) and plasma display panels and also applied devices thereof, and more particularly, to a flat display device having such a configuration that a display body module and a display control unit for controlling the display are separately disposed as well as to a display body driving device.

2. Background Art

A portable personal computer and word processor known as a so-called laptop type generally have hitherto incorporated an opening/closing type flat display unit. Middle-and-large-sized liquid crystal display devices mounted therein each consist of, as illustrated in FIG. **9**, a liquid crystal display unit **10** built into the device body and a flat liquid crystal display module unit **20** provided inwardly of an opening/closing cover so that these units are separately independently disposed. The liquid crystal display control unit **10** includes a liquid crystal module controller **12** and a microprocessor unit (MPU), not shown. The liquid crystal module controller **12** supplies a variety of control signals and clock signals to liquid crystal display module unit **20**. The liquid crystal display module unit **20** has:, e. g., a simple matrix type liquid crystal display panel (matrix liquid crystal display elements) **22**; a signal electrode driving circuit (X drivers) **24** and a scan electrode driving circuit (Y drivers) **26** which are TAB-packaged in peripheral regions (frame) of the panel **22**; and a liquid crystal power source circuit **28** for generating high liquid crystal driving voltages (reference voltages) V_0–V_5. Signal electrode driving circuit **24** is composed of a plurality of signal electrode driver semiconductor integrated circuits 24_1–24_m which are cascade-connected. Signal electrode driving circuit **24** supplies driver outputs per picture line to, e. g., M-pieces of signal electrodes in total. More specifically, data signals D0–D7 are sequentially taken in a shift register within the signal electrode driving circuit **24** by pixel clocks (shift clock pulses) XSCL. When the signals (M bits) per picture line are taken in, the data signals within the shift register are transmitted in parallel to a data latch circuit by scan line synchronous signals (data signal latch clocks LP) YSCL. The data signals undergo series/parallel conversion. The data latch circuit holds a signal voltage per line during a 1-scan period. Based on this signal voltage, a selection switch circuit sets output voltages of drivers connected to the signal electrodes either in a selection state or in a non-selection state. The AC-transforming clock FR is a clock for transforming each voltage described above into an AC waveform in order to prevent a deterioration of the liquid crystal elements due to a DC drive. A forced blank display signal DF is conceived as a signal for forcibly bringing a liquid crystal picture into a blank display state. The scan electrode driving circuit **26** consists of a plurality of scan electrode driver semiconductor integrated circuits 26_1–26_n which are cascade-connected.

The circuit **26** works to give a section voltage to only one of a total of N pieces of scan electrodes and non-selection voltages to the rest of them, i. e., (N −1) pieces of scan electrodes. A 1-scan line period is started by the scan start pulse (frame start signal) SP. Every time a scan line synchronous signal YSCL (data signal latch clock LP) comes, the selection voltages are sequentially impressed on the scan electrodes from the first line electrode to the N-th line electrode (line sequence display). The liquid crystal power source circuit **28** disposed on the side of the liquid crystal display module unit **20** generates a plurality of liquid crystal driving voltages V_0–V_5 selected by the selection switch of the scan electrode driving circuit **26** and the signal electrode driving circuit **24**. The liquid crystal power source circuit **28** is set in power on/off states by the forced blank display signal DF.

The liquid crystal display control unit **10** built in the device body is connected to the flat liquid crystal display module unit **20** typically through a hinge-connected movable part by using a flexible cable **30**. With this arrangement, the cable **30** itself is bent every time the opening/closing cover on the side of the flat liquid crystal display module unit **20** is opened and closed. Signal lines of the cable **30** tend to be damaged or disconnected due to physical factors. If a part of the signal lines are disconnected, there arises a situation where no AC drive is effected in such a state that a DC voltage (DC component) remains impressed on, e. g., a liquid crystal display panel **22**. Deterioration of the liquid crystal display panel **22** is caused which is more expensive than other parts and therefore difficult to exchange. This liquid crystal deterioration is conceived as a factor of obstacle to display quality and life-span. This is a serious problem to the display device based on visual recognizability. Among the signals supplied to the liquid crystal display module unit **20** from the liquid crystal module controller **12**, the signals which may induce a decline of the DC drive of the liquid crystal display panel **22** are a scan start pulse SP, a scan line synchronous signal YSCL (data signal latch clock LP), an AC-transforming clock FR, and a logic-side power source voltage Vcc. When some operational abnormalities occur in the liquid crystal module controller **12** and the microprocessor unit (MPU), abnormalities arise in the respective signals. There exists a possibility where the situation similar to the above-mentioned may take place.

Expanding the problem about the DC drive of the liquid crystal display body, this can be generalized to a problem associated with a signal abnormality on the side of the liquid crystal module unit. Besides, where a wall-mounted TV is presumed, because of a display control unit and a display panel being disposed in remote places, a problem in terms of deterioration in display quality is produced due to attenuation of signal level and the influence of noise as well as signal stoppage. Furthermore, problems also occur not only in liquid crystal displays but also plasma displays.

Accordingly, it is an object of the present invention devised in light of the above-described problems to provide a flat display device and a display body driving device which are capable of preventing deterioration of display characteristics due to a DC drive of a display panel, this deterioration being derived from an abnormality of a signal supplied from a display control unit to a display body module unit.

DISCLOSURE OF THE INVENTION

Generally in a flat display device wherein a display body module unit and a display control unit for controlling the

display thereof are separately disposed, the display body module unit performs passive operations while following up control signals given from the display control unit. The present invention, however, adopts an autonomous signal system including a signal management control means. All of the components of the signal management control means can be provided on the side of the display body module unit. Those components may, however, be disposed distributively on the side of the display body module unit and in the display control unit.

Such a signal management control means consists of a signal detection means for detecting an occurrence of abnormality of a first signal transferred from the display control unit and a sequence processing means for changing a signal mode on the side of the display body module unit on the basis of the output thereof. The signal abnormality implies signal stoppage, a shrinkage in logic amplitude and an interference. A typical example may be the signal stopping. A liquid crystal display device and a plasma display device may be exemplified as a flat display device. The signal detection means is composed concretely of a signal stop detection means for detecting a stop of a first signal. The sequence processing means is a forced stop control means for control-setting, to zero, a display body application voltage supplied to a display panel body of a display body driving means on the basis of the output thereof. When the first signal is stopped on the side of the display body module, this stop is detected by the signal stop detection means. The display body driving means is thereby controlled by the forced stop control means. The driving means sets the display body application voltage to zero. Hence, even when stopping the first signal such as a clock or the like, DC drive of the display body of the liquid crystal is avoided, thereby preventing deterioration of the display characteristics.

The following is an adoptable arrangement of the concrete forced stop control means. The forced stop control means includes a first signal delay means for delaying a second signal transferred from the display control unit by an output of the signal stop detection means. Display on/off of the display body driving means is controlled based on the output thereof. With such an arrangement, as a matter of course, the display on the liquid crystal panel can be quickly set in an off-state upon generating the detection signal. When the first signal resumes, however, the action is not that the display-on state is restarted at that moment but that the display body driving means is control-set in a display-on state after a time predetermined based on a cycle of the second signal has elapsed. Such a display body driving means control method, in terms of time difference, is capable of preventing an abnormal drive due to an abnormality of the power source, the abnormality being induced from a rush current. This control method is also capable of reducing a power source load and simplifying a power source circuit. The signal delay means receives a frame start signal as a second signal and is desirably N-staged D-type flip-flops settable and resettable, based on an output of the detection means. A delay time in such a case is determined on the unit of frame period. Another adoptable arrangement is that a plurality of signal management control means are disposed on the side of the liquid crystal module. In this case, it is possible to simultaneously detect plural kinds of signals. The forced stop control means is provided with a third signal control terminal for controlling the output thereof, whereby the plurality of signal management control means can be cascade-connected. In such a case, when any detected signal is stopped, display-off with respect to the display body driving means is controllable.

In order to further prevent deterioration of the display body due to the abnormal drive attributed to the rush current, it is desirable that the display body module be provided with a power source control means for controlling power on/off of a display body power source means for generating display body driving voltages. This power source control means controls power on/off of the display body power source means, corresponding to an output of the detection means. By this control process, after confirming an appearance of the first signal on the side of the display body module unit, the display body power source means is powered on. The following is an adoptable construction of the concrete power source control means. The power source control means includes a second signal delay means for delaying the second signal transferred from the display control unit by the output of the detection means. Based on the output thereof, power on/off of the display body power source means is controlled. With this arrangement, the output of the first signal is confirmed, and, after the time predetermined based on the cycle of the second signal has passed, the display body driving means is energized. For this reason, the power source control means receives an input of a display on/off signal as a second signal.

Where the power source control means is M-staged (<N) D-type flip-flops which are set/reset by an output of the detection means, after energizing the display body power source means, the display body driving means is put into a display-on state. This also contributes a reduction in the rush current. However, M and N are positive integers.

The signal management control means relative to the above-described construction is provided on a glass substrate on the side of the display body module unit. The signal management control means can be incorporated into a circuit of the display body driving device which is packaged on the side of the display body module unit. Namely, a display body driving means incorporating a signal management control function can be actualized. The conventional display body driving means is configured in the form of drivers LSI. The forgoing display body driving means with the signal management control function can be constructed as a semiconductor integrated circuit. Y drivers LSI among the drivers LSI are smaller in the number of I/O wires than X drivers LSI. Taking this fact into consideration, it is advantageous that the Y drivers are employed as the drivers LSI with the signal management control function. Liquid crystal display devices are classified roughly into a simple matrix type and an active matrix type. Drivers LSI with the signal management control function are desirably scan drivers or gate drivers.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram illustrating a whole configuration of a liquid crystal display device in an embodiment 1 of this embodiment;

FIG. 2 is a circuit diagram showing constructions of respective scan drivers and connective relations between drivers in the same embodiment;

FIG. 3 is a circuit diagram illustrating scan electrode driving cells of the scan driver in the same embodiment;

FIG. 4 is a timing chart, showing relations between a variety of signals in a liquid crystal display body module unit, of assistance in explaining the operation of the same embodiment;

FIG. 5 is a block diagram depicting a whole configuration of the liquid crystal display device in an embodiment 2 of this invention;

FIG. 6 is a circuit diagram showing constructions of the signal management control units of the respective scan drivers and connective relations between the drivers in the same embodiment;

FIG. 7 is a circuit diagram illustrating construction of a liquid crystal power source circuit in the same embodiment;

FIG. 8 is a timing chart, showing relations of a variety of signals in the liquid crystal display body module unit, of assistance in explaining the operation of the same embodiment; and

FIG. 9 is a block diagram depicting one configuration of a conventional liquid crystal display device.

BEST MODE FOR CARRYING OUT THE INVENTION

Embodiments of the present invention will hereinafter be described with reference to the accompanying drawings.

(Embodiment 1)

FIG. 1 is a block diagram illustrating a whole configuration of a liquid crystal display device in an embodiment 1 of this invention. Note that in FIG. 1, the same components as those of FIG. 9 are marked with the like reference symbols, and the description thereof will be omitted.

Signal management control units 47 are incorporated into scan driver semiconductor integrated circuits (LSI) 46_1–46_n combined to constitute a scan electrode driving circuit (Y drivers) of a liquid crystal display module unit **40** in this embodiment. A signal management control unit 47_1 of the first scan driver semiconductor integrated circuit 46_1 detects stoppage of a scanning line synchronous signal YSCL (data signal latch clock LP) applied to a terminal CKB1. The signal management control unit 47_2 of the second scan driver semiconductor integrated circuit 46_2 detects stoppage of a scan start pulse (frame start signal) SP applied to a terminal CKB2. A signal management control unit 47_n of the n-th (e.g., third) scan driver semiconductor integrated circuit 46_n detects stoppage of an AC-transforming clock FR applied to a terminal CKBn. The respective signal management control units 47_1–47_n have signal stop detection control terminals S_1–S_n and signal stop detection terminals T_1–T_n. A forced blank display signal DFF of a high level voltage is normally supplied from the control circuit **10** to the signal stop detection control terminal S_1 of the signal management control unit 47_1 of the first scan driver semiconductor integrated circuit 46_1. The signal stop detection terminal T_1 is connected to the signal stop detection control terminal S_2 of the signal management control unit 47_2 of the second scan driver semiconductor integrated circuit 46_2. The signal stop detection terminal T_2 of the signal management control unit 47_2 of the second scan driver semiconductor integrated circuit 46_2 is connected to a signal stop detection terminal (e. g., the signal stop detection control terminal S_n of the n-th signal management control unit 47_n) of the next stage. The signal stop detection terminal T_n of the n-th signal management control unit 47n is connected to forced blank control terminals DF of the scan drivers 46_1–46_n and the signal drivers 24_1–24_n.

The signal management control units 47_1–47_n of the respective scan drivers are, as illustrated in FIG. 2, cascade-connected. Configurations of the signal management control units 47_1–47_n are the same. A detected signal of the signal management control unit 47_1 is a data signal latch clock LP applied to the terminal CKB_1. A detected signal of the signal management control unit 47_2 is a scan start pulse (frame start signal) SP applied to the terminal CKB_2. A detected signal of the signal management control unit 47_n is an AC-transforming clock FR applied to the terminal CKBn.

Now, an emphasis is placed on the signal management control unit 47_1, and the construction thereof will be explained. The signal management control unit 47_1 includes a signal stop detection circuit **48** serving as a signal detection means for detecting stoppage of the detected signal and a sequence processing circuit **51** consisting of a signal delay circuit **49** and a logic circuit **50**.

The signal stop detection circuit **48** is composed of: a first N-type MOS transistor Tr_1 switched by a latch clock LP conceived as a detected signal and constituting a transfer gate; an inverter INV_1 for inverting a phase of the latch clock LP; a second N-type MOS transistor Tr_2 switched by an antiphase signal of the latch clock LP and constituting a transfer gate; a first capacitor C_{11} for effecting a charge and discharge in accordance with opening/closing operations of the first N-type MOS transistor Tr_1; a second capacitor C_{12} for effecting the charge and discharge in accordance with the opening/closing operations of the second N-type MOS transistor Tr_2; a discharge resistor R_1 for discharging an electric charge of the capacitor C_{12}; and an inverter INV_2 for outputting a charge level judgment signal by comparing a charge voltage of the second capacitor C_{12} with a threshold value V_{TH}. The first N-type MOS transistor Tr_1, the inverter INV_1 and the second N-type MOS transistor Tr_2 are combined to constitute a series exclusive keying circuit. The first N-type MOS constitutes a selective charge switch for the first capacitor C_{11}. The second N-type MOST transistor Tr_2 constitutes a selective charge switch for distributively transferring a charge of the first capacitor C_{11} to a second capacitor C_{12}.

The signal delay circuit **49** consists of: a D-type flip-flop **49***a*, in which the frame start signal SP serves as a clock input CK, including a reset terminal R connected to an output of the inverter INV_2 and an input terminal D earthed; and a D-type flip-flop **49***b*, in which the frame start signal SP serves as a clock input, including a reset terminal R connected to the output of the inverter INV_2 and an input terminal D connected to an output Q of the flip-flop **49***a*. The logic circuit **50** is constructed of an AND circuit which receives two inputs of the forced blank signal DFF from the control circuit **10** and an output Q of a flip-flop **49***b*.

FIG. 3 is a circuit diagram illustrating a typical scan electrode driving circuit (logic unit) other than the signal management control unit 47_1 of the scan driver 46_1. Formed in array in this logic unit are multi-bit scan electrode driving cells 46_{11}, 46_{12}, . . . for applying voltages in the order of lines corresponding to a multiplicity of scan electrodes. Turning to FIG. 3, there are illustrated the scan electrode driving cells 46_{11}, 46_{12} of the first and second bits and peripheral circuits thereof.

Attention is herein paid on the scan electrode driving cell 46_{11}, and its configuration will be explained. This scan electrode driving cell 46_{11} consists of: a D-type flip-flop **46***a*, in a shift register, started by the frame start signal SP and transferring this frame start signal SP to the next stage every time a scan synchronous signal YSCL comes; a line unit forced blank display control circuit **46***b* for performing a logic arithmetic operation by adding, to its bit selection output Q, a forced blank display signal DF supplied from the terminal T_n of the n-th scan driver **46***n*; a line unit voltage level shift circuit **46***c* for converting an output thereof into a high voltage system logic amplitude from a logic system power source voltage (V_{cc}=5v); a total line forced blank display control circuit **46***d* for performing a logic arithmetic operation by adding the forced blank display signal DF to the AC-transforming clock FR; an AC-transforming clock voltage level shift circuit **46***e* for converting the

AC-transforming clock FR into a high voltage AC-transforming clock F_{RH} having a high voltage system logic amplitude from the logic system power source voltage (V_{cc}=5v); a positive/opposite 2-phase clock generation circuit **46***f* for inverting the high voltage AC-transforming clock FR_H thereof to an antiphase high voltage AC-transforming clock FR_H; a selection control signal generation circuit **46***g* for generating four pieces of selection control signals C_1–C_4 in chained combinations from a pair of the high voltage AC-transforming clock FR_H and the antiphase high voltage AC-transforming clock F_{RH} and a pair of outputs **0**, **0** of the line unit voltage level shift circuit **46***c*; and a selection switch **46***h* for alternatively convey-supplying scan electrode driving voltages V_5, V_1, V_0, V_4 to the scan electrodes in response to respective selection control signals C_1, C_2, C_3, C_4. A forced blank display control circuit is herein composed of the line unit forced blank display control circuit **46***b* and the total line blank display control circuit **46***d*. Note that the symbol INV_3 represents an inverter for matching logic with respect to the line unit forced blank display control circuit **46***b* of the forced blank display control signal DF.

Next, the operation of this embodiment will also be explained with reference to FIG. **4**. When turning on a logic power source V_{cc} of the liquid crystal display device at a time t_0, a reset signal having a pulse width of several μs—several ms is supplied to a power-on reset terminal RS of a liquid crystal module controller **12** from an MPU (not illustrated) in the same manner with the prior art. The liquid crystal module controller **12** is thereby initialized. During this initialization, a variety of signals outputted from the liquid crystal module controller **12** are generally in a stopping status. During this period, the forced blank display signal DFF assumes a low voltage level (hereinafter referred to as an L level). Hence, a liquid crystal power source circuit **28** is in a power-off state, while the liquid crystal driving power source voltages V_0–V_5 remain in a non-generated state. Therefore, during this initialization, no DC component is applied between the liquid crystal electrodes, and deterioration in liquid crystal elements is prevented.

If over this period, as illustrated in FIG. **4**, the forced blank display signal DFF changes from the L level to a high voltage level (hereinafter referred to as an H level) at a time t_1, the liquid crystal module controller **12** generates the frame start signal SP, the data signal latch clock LP, and the AC-transforming clock FR. Now, the operation of the signal management control unit 47_1 of the scan driver 46_1 will first be described. The frame start signal SP is supplied to an input terminal CKA_1 of the signal delay circuit **49**. The data latch clock LP is supplied to a detection terminal CKB_1 of the signal stop detection circuit **48**.

During an H-level period of the data signal latch clock LP, the transistor Tr_1 of the signal stop detection circuit **48** assumes an on-status, whereas the transistor Tr_2 assumes an off-status. Hence, the capacitor C_{11} is charged with electricity for this period. During an L level period of the data signal latch clock LP, the transistor Tr_2 of the signal stop detection circuit **48** is in the on-status, whereas the transistor Tr_1 is in the off-status. Therefore, a part of the electric charge supplied to the capacitor C_{11} is transferred to a capacitor C_{12}. A charging voltage of the capacitor C_{12} increases with a generation of repetitive pulses of the data signal latch clocks LP. An input voltage of the inverter INV_2 comes to the threshold value V_{TH} or less. An output INV_{OUT} of the inverter INV_2 assumes the H level at a time t_2. Before the time t_2, the output INV_{OUT} of the inverter INV_2 assumes the L level. Therefore, the output Q of the D-type flip-flop **49***a* of the signal delay circuit **49** is at the L level. For this reason, an output T_1 of the logic circuit **50** assumes the L level. Even when the output INV_{OUT} becomes the H level at that moment, the output Q does not assume the H level at the time t_2. During a 1-frame period (T_F) and a 2-frame period ($2T_F$) of the frame start signal SP, the output Q is kept at the L level due to delayed storage action of the input signals of the D-type flip-flops **49***b*, **49***a*. At a time t_3, the output T_1 of the logic circuit **50** assumes the H level.

The frame start signal SP is supplied to the detection terminal C K B $_2$ of the signal stop detection circuit 48_2 of the signal management control unit 47_2 Supplied to an input terminal CKA_2 of the signal delay circuit 49_2 is the frame start signal SP defined as a cascade input DI_2 coming from a cascade output terminal D0 of the scan driver 46_1. The output T_1 of the logic circuit **50** of the scan driver 46_1 is cascade-connected to the logic circuit **50** of the scan driver 46_2. A capacitor C_{21} of the signal stop detection circuit 48_2 is fed with electric energy by repetitive pulses of the frame start signals SP. Similarly, the AC-transforming signal FR is supplied to a detection terminal CKBn of the signal stop detection circuit **48***n* of the signal management control unit **47***n* in the scan driver **46***n*. Supplied to an input terminal CKAn of the signal delay circuit **49***n* is the frame start signal SP defined as a cascade input DI_n coming from the output terminal D0 of the scan driver 46_2. The output T_2 of the logic circuit **50** of the scan driver 46_2 is cascade-connected to the logic circuit **50** of the scan driver **46***n*. A capacitor C_{n2} of the signal stop detection circuit **48***n* is charged with electricity by the repetitive pulses of the AC-transforming signals FR. The different periods and duty ratios of the data signal latch clock LP conceived as a detected signal, the frame start signal SP and the AC-transforming signal FR. For making coincident the comparative judgment times t_3 of the inverters INV_1–INV_n in the respective scan drivers, it is desirable that values (time constants) of discharge resistances R_1–R_n and of the capacitors C_{11}–C_{n1}, C_{12}–C_{n2} be mutually adjustable. For this purpose, in this embodiment, as illustrated in FIG. **1**, the scan driver is provided with external connection terminals for the resistances and the externally attached capacitors.

As described above, during a period from the on-time t_0 of the logic power source V_{cc} to the time t_3 when the outputs T_1–T_n of the logic circuit assume the H level, the L level outputs T_n are supplied to the forced display blank control terminals DF of the signal drivers and the scan drivers. A liquid crystal display panel **22** is therefore in a blank display state. More specifically, when the forced display blank control signal DF is at the L level, only a transistor F_1 of the selection switch **46***h* of the scan electrode driving cell **46** remains in an on-state under control of the forced blank display control circuits **46***b*, **46***d* depicted in FIG. **3**. A voltage of V_5 (0v) is impressed on the scan electrodes, while an inter liquid crystal electrode voltage (liquid crystal applying voltage) is 0v. A period from the time t_0 to the time t_3 corresponds to a liquid crystal drive inhibit period. At time t_1, the liquid crystal power source circuit **28** is powered on, whereby the liquid crystal voltages V_0–V_5 are generated. Those voltages are supplied to the scan and signal drivers. At a power source actuation time, the shift registers in the scan and signal drivers are in an unsteady state. The liquid crystal display continues to be blank-controlled up to the time t_3, however, it is therefore possible to avoid abnormal driving of the liquid crystal panel.

Next, when the output T_n becomes the H level at the time t_3, H-level voltages are supplied to the forced display blank control terminals DF of the scan and signal drivers. The

liquid crystal display panel **22** is thereby AC-driven by normal operations of the scan and signal drivers. A display picture is depicted on the liquid crystal panel **22**. The symbol B of FIG. **4** indicates a liquid crystal driving period. The liquid power source circuit **28** and the logic units of the scan and signal drivers are powered on at the time t_1. At time t_3 later than that time, the liquid crystal display panel **22** is driven. Therefore, since the power-on of the power source does not take place simultaneously, an excessive power source rush current is restrained. It is because, in addition to delayed action of the signal stop detection circuit **48** itself, the delayed action of the signal delay circuit **49** having a delay time of 1–2 frame periods functions effectively.

Now, it is presumed that an output of the data signal latch clock LP transmitted from the liquid crystal module controller **12** is stopped at a time t_4 in the liquid crystal driving period B. During outputting of the data signal latch clock LP, sufficient electric energy is supplied to the second capacitor C_{12} of the signal detection circuit 48_1 of the scan driver 46_1. When the clock thereof is stopped, no electric charge is transferred to the second capacitor C_{12} from the first capacitor C_{11}. Besides, the electric charge of the second capacitor C_{12} is quickly discharged at a predetermined time constant via the discharge resistance R_1. An input voltage of the inverter INV_2 is gradually boosted. If that input voltage exceeds the threshold value V_{TH}, the output voltage INV_{OUT} thereof assumes the L level at a time t_5. With this logic variation, the signal delay circuit 49_1 is reset, and the output Q thereof becomes the L level. Hence, in spite of the fact that the forced display blank control signal DF is at the L level, the output T_1 of the logic circuit 50_1 assumes the L level at the time t_5. This T_1 output is cascade-inputted to the logic circuit 50_2 of the scan driver 46_2. Even when the frame start signal SP is being outputted, and output T_2 of the logic circuit 50_2 becomes the L level. Further, the T_2 output is cascade-inputted to the logic circuit 50_n of the scan driver **46***n*. Therefore, the output T_n of the logic circuit 50_n assumes the L level even when the AC-transforming signal FR is being outputted. The output T_n thereof corresponds to the forced display blank control signal DF on the side of the liquid crystal display module unit **46**. The liquid crystal panel **22** is thereby brought into a blank display state by using the forced display blank circuits **46***b*, **46***d*. Namely, only a transistor F_1 of the selection switch **46***h* of the scan electrode driving cell **46** shown in FIG. **3** is in the on-state. A voltage V_5 (**0**v) is fed to the scan electrodes, and the inter liquid crystal electrode voltage is thereby kept at **0**v. For this reason, even if the data signal latch clock LP is stopped due to some cause, the liquid crystal elements are not driven by the DC components, thereby preventing deterioration of the liquid crystal beforehand. If the frame start signal SP or the AC-transforming signal FR is stopped due to some cause, the output T_n becomes the L level. Similarly, the deterioration of the liquid crystal is prevented beforehand. Incidentally, during this liquid crystal drive inhibit period A, so far as the frame start signal SP and the AC-transforming signal FR continue, the second capacitor C_{22} and the capacitor C_{n1} are in a charged state; and the outputs of the inverters INV_2, INV_n assume the H level.

When the data signal latch clock LP begins to reappear at a time t_6, as described above, the second capacitor C_{12} is charged with electricity. The output INV_{OUT} of the inverter INV_1 then becomes the H level. After 1–2 frame periods from the time when the output INV_{OUT} has become the H level, the output Q of the signal delay circuit 49_1 functioning as a timer assumes the H level at a time t_7. The output T_1 of the logic circuit 50_1 thereby becomes the H level, and correspondingly the outputs T_2, T_n of the logic circuits 50_2, 50_n become the H level. Hence, the forced blank control signal DF on the part of the liquid crystal module unit **22** is changed to the H level, whereby the liquid crystal display panel **22** enters the liquid crystal driving period B.

Finally, when the forced display blank control signal DFF on the part of the liquid crystal display controller **12** assumes the L level at a time t_8, the output T_1 of the logic circuit 50_1 is changed to the L level. The outputs T_2, T_n of the logic circuits 50_2, 50_n thereby become the L level. Therefore, the forced display blank control signal DF on the side of the liquid crystal display module unit **20** becomes the L level. The liquid crystal display panel **22** enters a display-off period C.

(Embodiment 2)

FIG. **5** is a block diagram illustrating the liquid crystal display device in an embodiment 2 of this invention. Note that in FIG. **5**, the same components as those of FIG. **1** are marked with like reference symbols, and the description thereof will be omitted.

A scan electrode driving circuit (X drivers) of a liquid crystal display module unit **70** is composed of a plurality of scan drivers 76_1–76_n. These scan drivers include signal management control units 77_1–77_n identical with the signal management control units of the embodiment 1. Added to the respective signal management control unit 77_1–77_n, as illustrated in FIG. **6**, are power source power on/off control circuits 78_1–78_n for controlling power on/off times of the liquid crystal power source circuit **28** for generating the liquid crystal driving voltages V_0–V_5. Each of the power source power on/off control circuits 78_1–78_n is constructed of: an inverter INV_3 for inverting signals coming in input terminals S_1–S_n of the logic circuit 50_n; 2-stage-connected D-type flip-flops **78***a*, **78***b*; and a logic circuit **78***c* for taking logic with respect to the signals coming from terminals P_1–P_n and the output Q. A signal delay circuit **79** of each signal management control unit **77** is constructed in such a way that a D-type flip-flop **79***c* of the third stage is additionally connected to the 2-stage-connected D-type flip-flops **49***a*, **49***b* of the signal delay circuit **49** in the embodiment 1. A power on/off signal of the power source voltage V_{cc} on the logic side is supplied to an input terminal P_1 of a logic circuit **78***c* of the first scan driver 76_1. An output PF_1 of the power source power on/off control circuit 78_1 in the first scan driver 76_1 is cascade-supplied to a terminal P_2 of the second scan driver 76_2. An output PF_2 of the power source power on/off control circuit 78_2 in the second scan driver 76_2 of the previous stage, is cascade-supplied to a terminal P_n of the n-th scan driver 76_n. An output PF_n of the power source power on/off control circuit **78***n* of the n-th scan driver **76***n* is supplied to a power-off terminal POFF of the liquid crystal power source circuit **28**.

The liquid crystal power source circuit **28** is structured in the same way with the conventional example. This circuit, as depicted in FIG. **7**, includes: a voltage transforming circuit **28***a* for generating a high voltage (20–40v) which is boosted based on the V_{cc} (5v) power source voltage; an npn-type transistor **28***b* for effecting on/off control depending on a value of the voltage supplied to the power-off terminal POFF; a pnp-type transistor **28***c* of a power switch for performing on/off operations interlocking with on/off operations of the transistor **28***b*; a smoothing capacitor **28***d* interposed between a collector thereof and the earth; and a voltage dividing circuit **28***e* for outputting the liquid crystal driving voltages V_0–V_5 from the charge voltage thereof.

The operation of the foregoing embodiment will next be explained with reference to FIG. **8**. A power switch SW is

closed at a time t_0. The logic power source V_{cc} of the liquid crystal display device is turned on. In the same manner as embodiment 1, a reset signal having a pulse width of several μs—several ms is supplied from an MPU to a power-on reset terminal RS of the liquid crystal module controller **12**. The liquid crystal module controller **12** is thereby initialized. Hence, an output signal from the liquid crystal module controller **12** is generally in a stopping status. During such a period, the logic power source voltage V_{cc} is supplied to one input of the logic circuit **78***c* defined as an AND circuit of the first scan driver 76_1. The data signal latch clock LP does not yet, however, come out, and hence its output PF_1 assumes the L level. As a result, an output PF_2 of the second scan driver 76_2 is also at the L level. Besides, an output PE_n of the n-th scan driver 76_n also becomes the L level, whereby a power-off terminal POFF of the liquid crystal power source circuit **28** is kept at the L level. For this reason, a base potential of the transistor **28***b* shown in FIG. **7** assumes an L level (0v), so that a boosted voltage is not supplied to the smoothing capacitor **28***d*. Therefore, the liquid crystal driving voltages V_0–V_5 are not generated. As is similar to embodiment 1, no DC component is applied between the liquid crystal electrodes during this initializing period. Deterioration of the liquid crystal elements is prevented.

Next, as illustrated in FIG. **8**, a variety of signals are generated from the liquid crystal module controller **12** at a time t_1. The forced blank display signal DFF is changed from the L level to the H level. The frame start signal SP, the data signal latch clock LP, and the AC-transforming clock FR are generated. As explained in embodiment 1, upon the data signal latch clock LP starting to appear, the output INV_{OUT} of the inverter INV_2 assumes the H level at a time t_2. For this reason, the output Q of the power on/off control circuit **78***b* becomes the H level at a time t_3 which is later by a 1–2 frame period than the time t_2. The output PF_1 of the logic circuit **78***c*, therefore, becomes the H level. The outputs PF_2, PFn of the logic circuits **78***c* of the second and n-th scan drivers 76_2, 76_n become the H level, correspondingly. The power-off terminal POFF of the liquid crystal power source circuit **28** is energized at the H level. In consequence of this, the transistor **28***b* is put into an on-state. The transistor **28***c* is also brought into the on-state because of a drop in voltage of an inter base/emitter resistance of the transistor **28***c*. The smoothing capacitor **28***d* is charged with electricity, thereby generating the liquid crystal driving voltages V_0–V_5. During a period from the time t_3 to a time t_4 when the next frame start signal SP arrives, the output Q of the D-type flip-flop **79***c* remains at the L level. The stage number of the D-type flip-flops of the signal delay circuit 79_1 in this embodiment is greater by 1 than in the power on/off control circuit 78_1. The output Q of the D-type flip-flop **79***c* becomes the H level, but slower by a 1-frame period T_F than that of the D-type flip-flop **78***b*. As a result, the outputs T_{11}, T_{27}, Tn all become the H level. In the same manner as embodiment 1, the forced blank display signal DF on the part of the liquid crystal module unit is changed from the L level to the H level. The driving voltages V_0–V_5 are thereby supplied to the scan and signal electrodes of the liquid crystal display panel **22**. The operation then enters a liquid crystal mode.

For instance, concurrently with generation of the liquid crystal driving voltages V_0–V_5, the liquid crystal display panel **22** is driven. It follows that large charge rush currents are induced in power source units of the scan and signal drivers as well as in the liquid crystal panel. In accordance with this embodiment, however, the liquid crystal drive is initiated after the 1-frame period T_F since the liquid crystal driving voltages V_0–V_5 have been generated at the time t_3. The power source units are energized with a time difference, whereby the rush currents can be dispersed. This makes it possible to prevent a power-down and reduce power capacity, which is in turn helpful for protecting the liquid crystal display panel and the drivers as well. The above-described power control decreases burden in terms of system development costs and restrains an increase in the number of signal wires between the conventional system and LCD module. Furthermore, a reduction in power capacity is brought about, and hence inexpensive power source is available.

Next, supposing that oscillations of the data signal latch clocks LP transmitted from the liquid crystal module controller **12** are stopped at the time t_5 in the liquid crystal driving period B, as in embodiment 1, the input voltage of the inverter INV_2 is boosted. The output voltage INV_{OUT} becomes the L level at a time t_6. The outputs T_1, T_2, T_n also become the L level. As a result, the forced display blank control signal DF on the side of the liquid crystal display module unit assumes the L level. The liquid crystal display panel **22** is thereby put into a blank display state. The effects as those of embodiment 1 are exhibited. When the output voltage INV_{OUT} of the inverter INV_2 assumes the L level, the outputs PF_1, PF_2, PF_n simultaneously become the L level. The power-off terminal POFF of the liquid crystal power source circuit **28** is changed to the L level. The liquid crystal driving voltages V_0–V_5 cease to be generated.

The data signal latch clock LP starts reappearing at a time t_7. In the same manner as embodiment 1, the output voltage INV_{OUT} of the inverter INV_2 becomes the H level at a time t_8. As discussed above, the outputs PF_{11}, PF_2, PF_n also become the H level at a time t_9 after a 1–2 frame period from time t_8. In consequence of this, the power-off terminal POFF of liquid crystal power source circuit **28** is changed to the H level. The liquid crystal driving voltages V_0–V_5 which are in turn applied to the drivers are generated. As explained earlier, the outputs T_1, T_2, T_n become the H level at a time t_{10} which is later by 1-frame period, T_F, than the time t_9. The liquid crystal driving voltages V_0–V_5 are supplied to the scan and signal electrodes of the liquid crystal display panel **22**. Then the liquid crystal resumes display mode.

When the forced display blank control signal DFF on the part of the liquid crystal display controller **12** becomes the L level at a time t_{11}, the outputs T_1, T_2, T_n also become the L level. Correspondingly, the forced display blank control signal DF on the side of the liquid display module unit **70** assumes the L level. The liquid crystal display panel **22** enters a display-off period C. At a time t_{12} after a 1–2 frame period from time t_{11}, the output Q of the D-type flip-flop **78***b* of the power on/off control circuit 78_1 is changed to the L level. The outputs PF_1, PF_2, PF_n also become the L level. As a result, the power-off terminal POFF of the liquid crystal power source circuit **28** also assumes the L level. Then the generation of the liquid crystal driving voltages V_0–V_5 stops. As described above, the forced display blank control signal DE on the side of the liquid crystal display controller **12** becomes the L level, after stopping the liquid crystal drive, and after a constant period has elapsed, no voltage is applied to the liquid crystal drivers. Relations in potential with respect to the logic power source V_{cc} and the liquid crystal driving voltages V_0–V_5 are maintained by the sequence during such a power-off period. A through current and a parasitic bipolar current within the driver are restrained, thereby protecting the liquid crystal display panel and the drivers as well.

In accordance with this embodiment, after the clocks have been supplied to the liquid crystal module, the liquid crystal